2010 January Semester
Mid-term Examination

INFT13-600 and 73-600
Special Topic in IT

Instructions to the Candidate
THESE INSTRUCTIONS RELATE TO THE ENTIRE EXAM.

1. Write your name or student-id in the space provided below.
2. Do not begin reading the questions until instructed.
3. There are several questions worth various marks.
4. Answer all questions on separate paper.
5. Return the Examination Paper and your answers to the exam supervisor at the end of the examination.

Student Name or ID: _____

Question 1 - Multiple Choice [5 marks]

For each question, circle the single correct answer.

1. Every boolean expression of N inputs and one output can be implemented
   (a) using a combination of D flip-flops, multiplexors and registers.
   (b) by connecting the output directly to all of the N inputs.
   (c) using a combination of And and Or gates.
   (d) using a combination of And, Or and Nand gates.

2. In twos-complement arithmetic, to create a negative value of a number X:
   (a) invert (Not) every bit in the number X.
   (b) invert the most significant bit of X.
   (c) add 1 to X, and invert every bit.
   (d) subtract 1 from X, and invert every bit.

3. In the HDL implementation of the Bit chip, the output from the DFF is connected to the input of the Mux. This is done
   (a) to convert the Mux into a sequential chip.
   (b) to ensure that the Bit value is retained after each clock cycle if load is off.
   (c) to ensure that the new input bit is stored on every clock cycle.
   (d) to ensure that the Bit value is retained after each clock cycle if load is on.

4. The A-instruction in the Hack computer performs
   (a) direct addressing.
   (b) immediate addressing.
   (c) indirect addressing.
   (d) bitwise addressing.

5. Each memory address in the Hack computer references
   (a) a single byte.
   (b) a single word.
   (c) multiple words.
   (d) the D-register.

..... /2.

Question 2 (5 marks)

The C-instruction in the Hack computer has the following structure:

```
1 1 1 a  c1 c2 c3 c4  c5 c6 d1 d2  d3 j1 j2 j3
```

where the *a* bit selects either the A-register or memory, the six *c* bits define what instruction is to be performed, the three *d* bits define the destination of the instruction result, and the three *j* bits define what jump operation (if any) should be performed.

Most computer architectures have the concept of a no-operation instruction, NOP, which has no effect on the state of the CPU except increment the program counter to address the next instruction. Find and write down a Hack C-instruction (i.e a specific pattern of 16 bits) which is equivalent to a NOP, i.e. which has no effect on the CPU except increment the program counter.

In your answer, explain why the instruction that you specified has no effect on the CPU state.

Question 3 (5 marks)

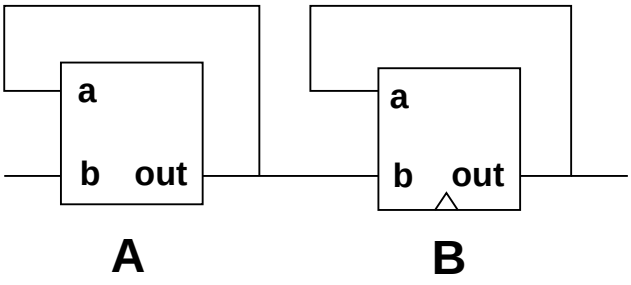
Estimate the number of NAND gates in:

1. a half-adder
2. a 16-bit full-adder

Show the working that you used to arrive at your estimates.

Question 4 (3 marks)

The following diagram shows a logic circuit using a combinatorial chip called A, and a sequential chip called B.



Explain why the wiring around chip B is legal, but the wiring around chip A is not legal.

Question 5 (7 marks)

The following gives the HDL interface definition of a chip called High4:

```
CHIP High4 {
  IN in[4];
  OUT out[2];
}
```

The purpose of the chip is to output a 2-bit integer that represents the number of the highest input bit which is on. For example, if in[2] is the highest input bit on, the output is 1,0; similarly, if in[1] is the highest input bit on, the output is 0,1. The full truth table for the chip is given below.

in[3]	in[2]	in[1]	in[0]	out[1]	out[0]
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Design a HDL implementation (or a logic circuit diagram) of the High4 chip which correctly implements the truth table. Also provide a short description of how your design implements the required functionality.

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